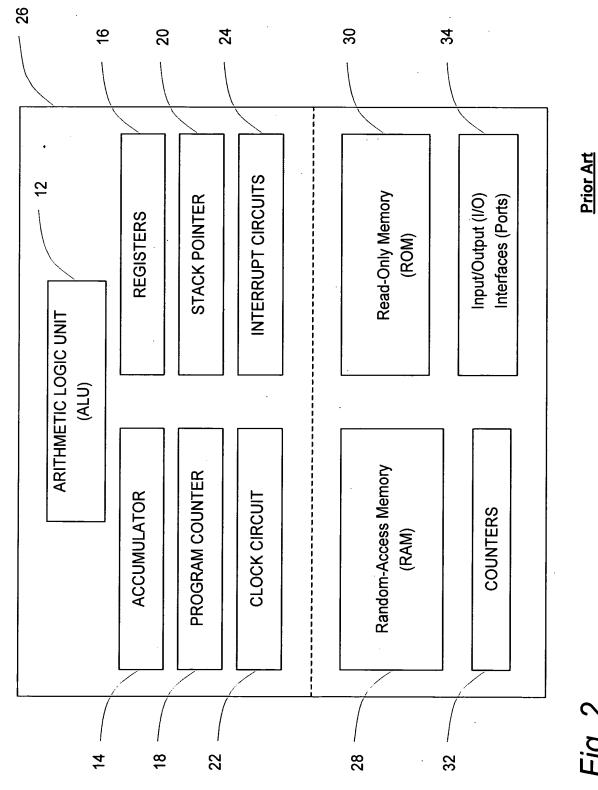


Prior Art

F1g. 1



F1g. 2

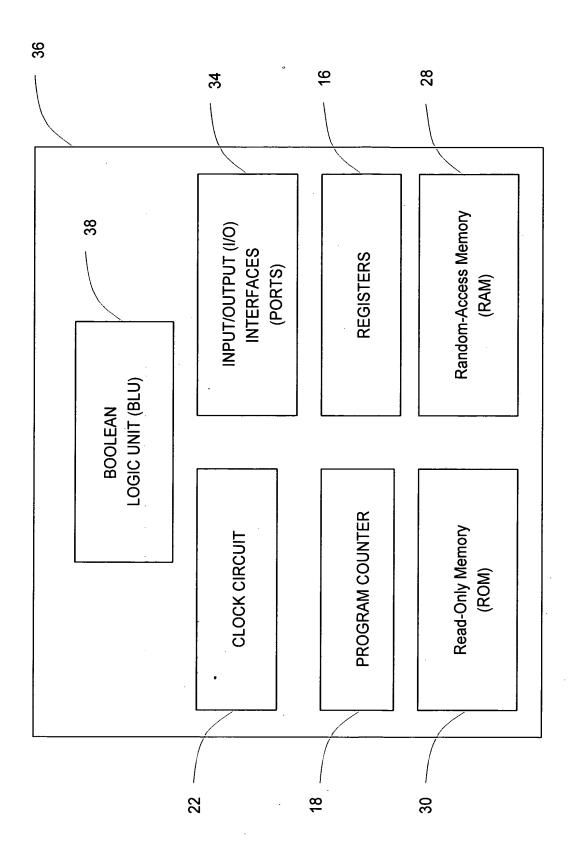
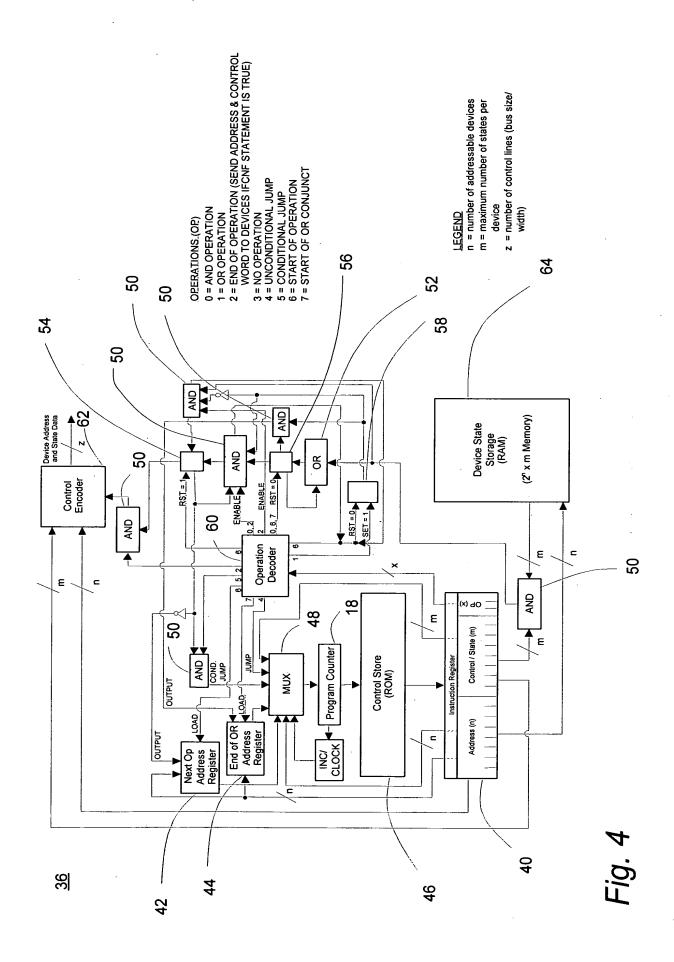


Fig. 3



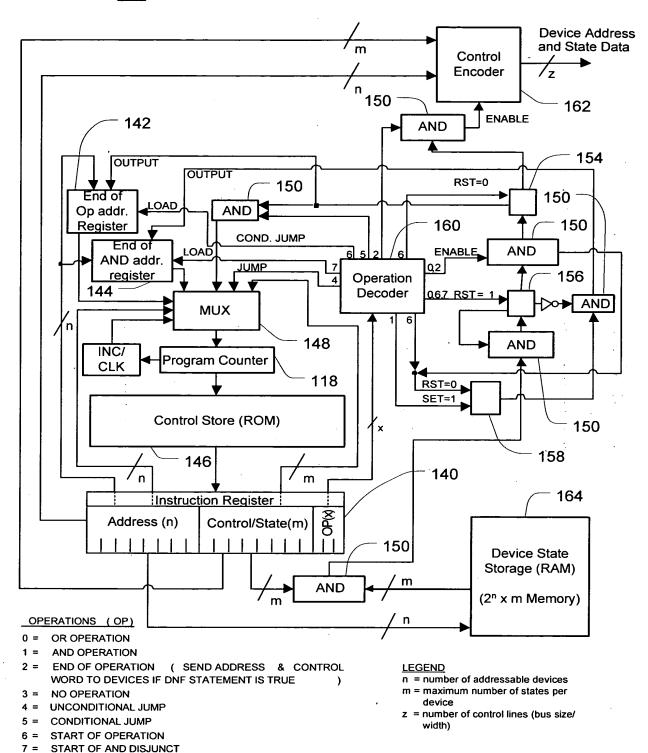


Fig. 5

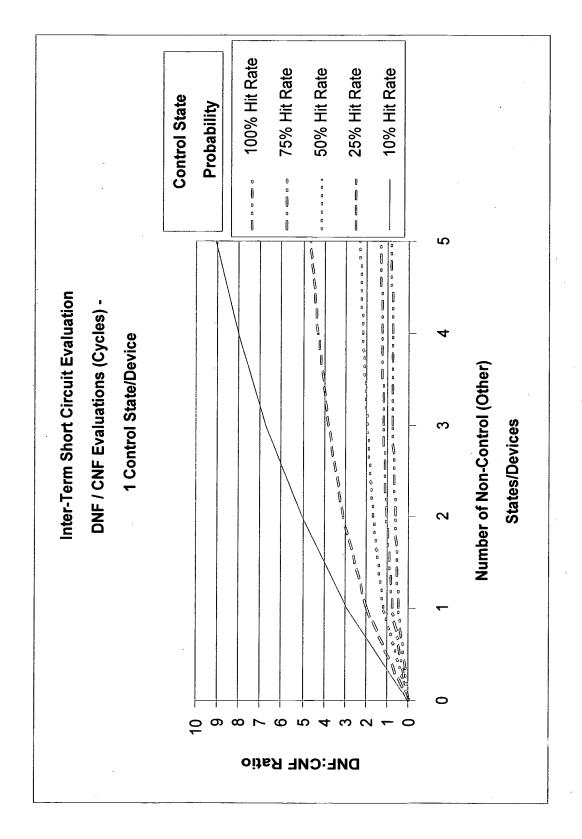


Fig. 6

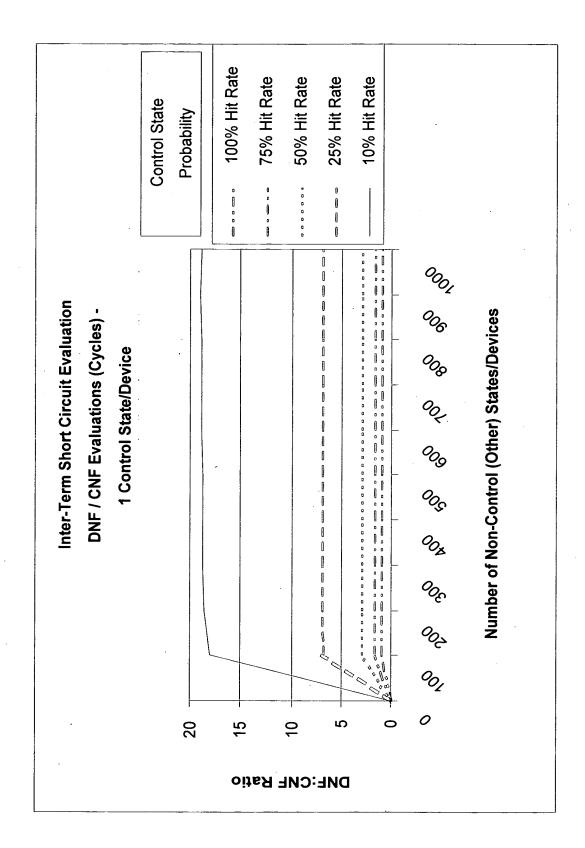


Fig. /

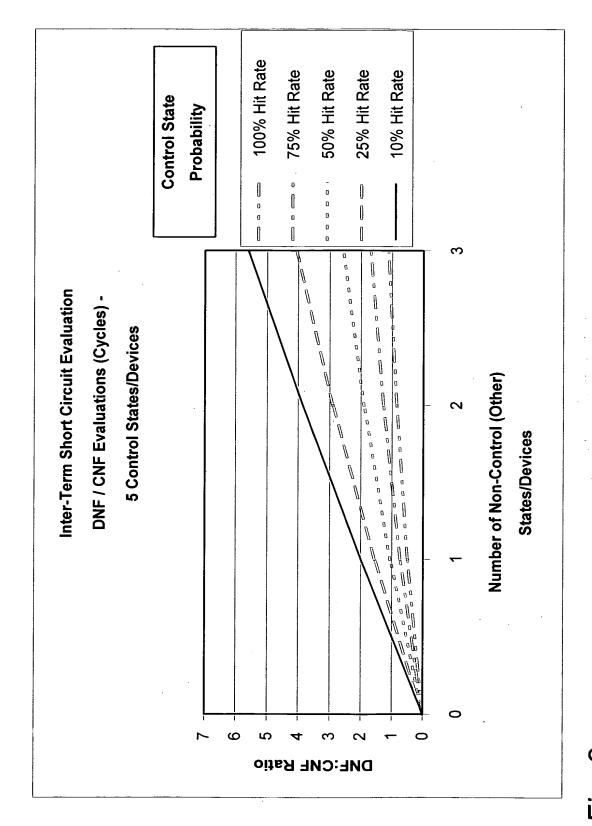


Fig. 8

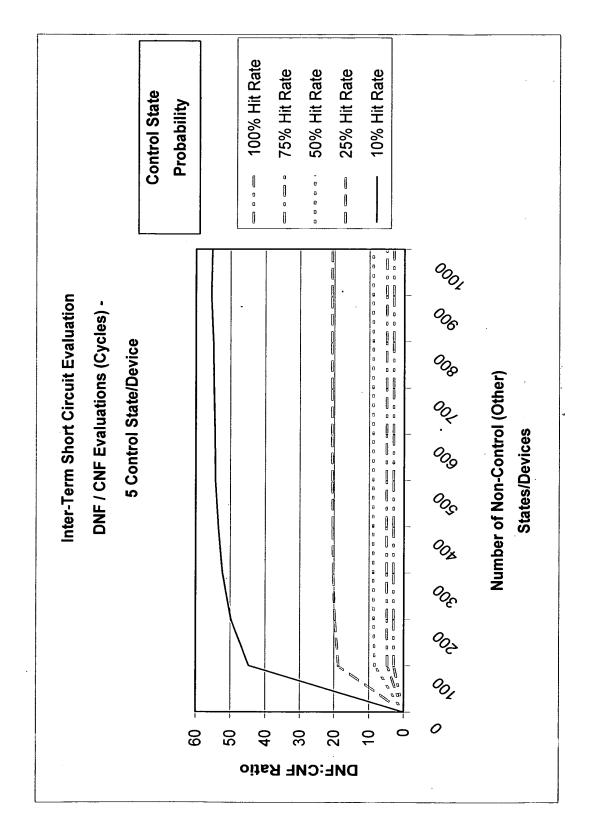


Fig. 9

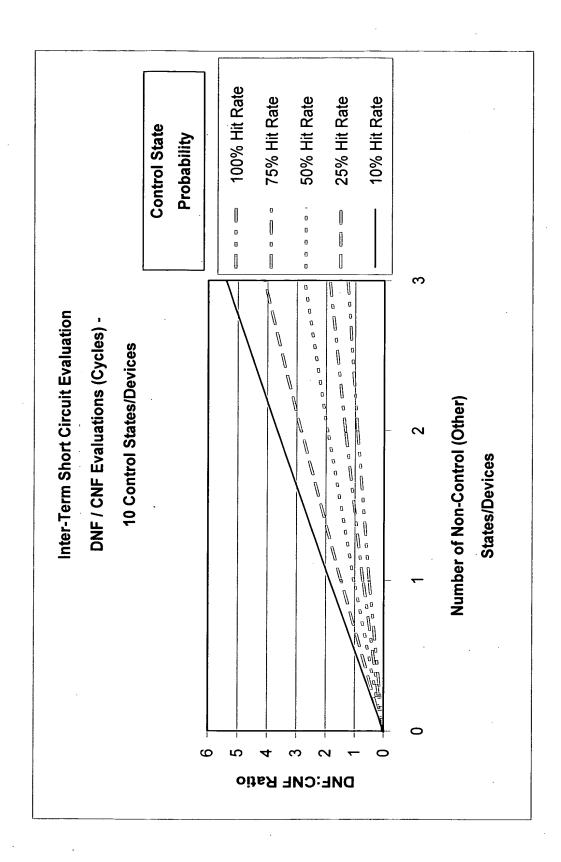


Fig. 10

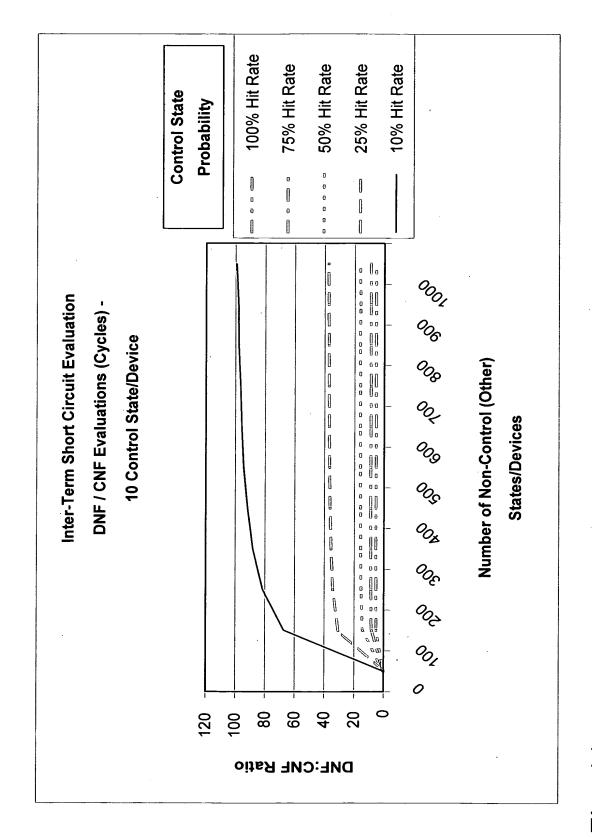


Fig. 11

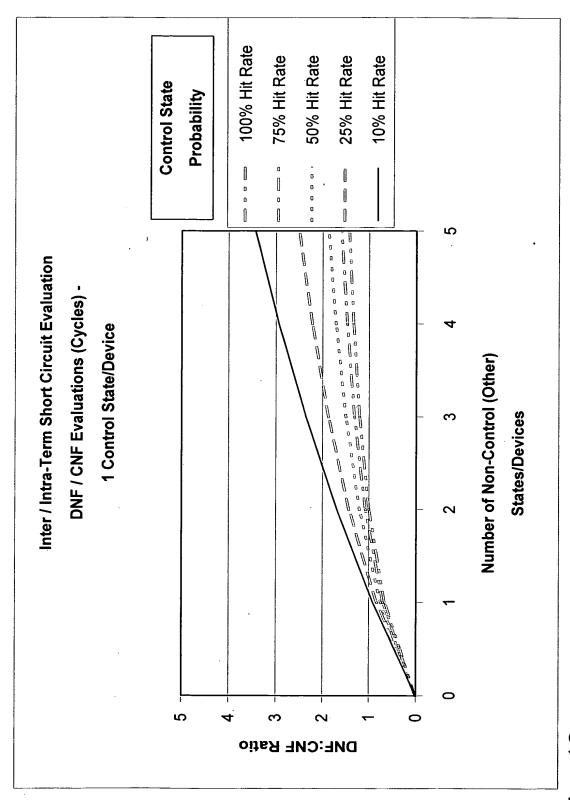


Fig. 12

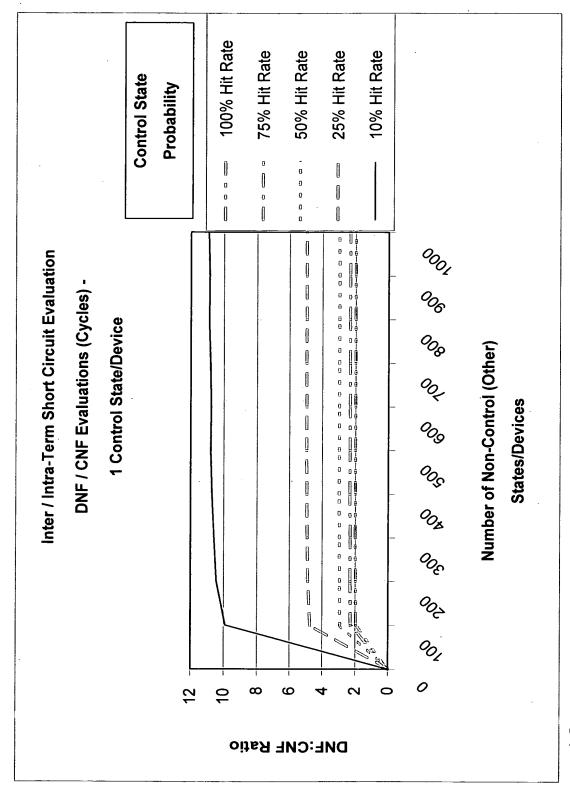


Fig. 13

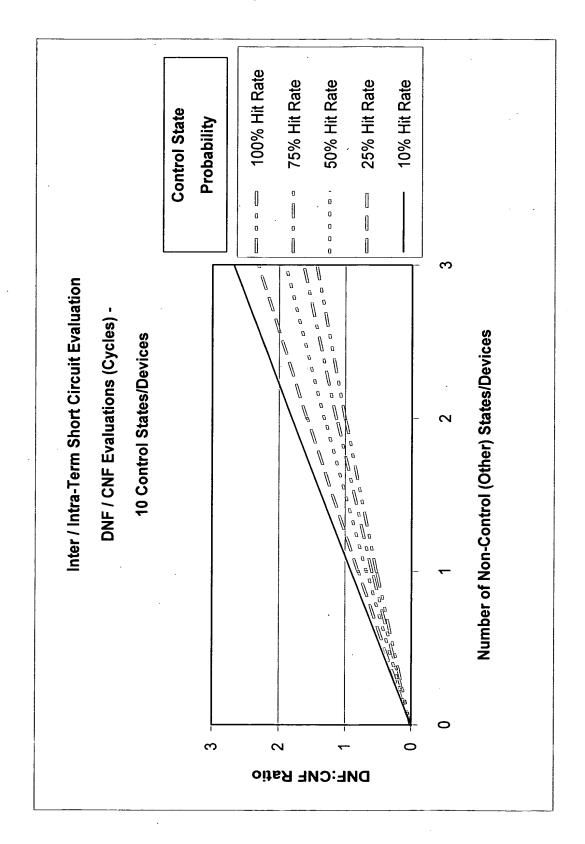


Fig. 14

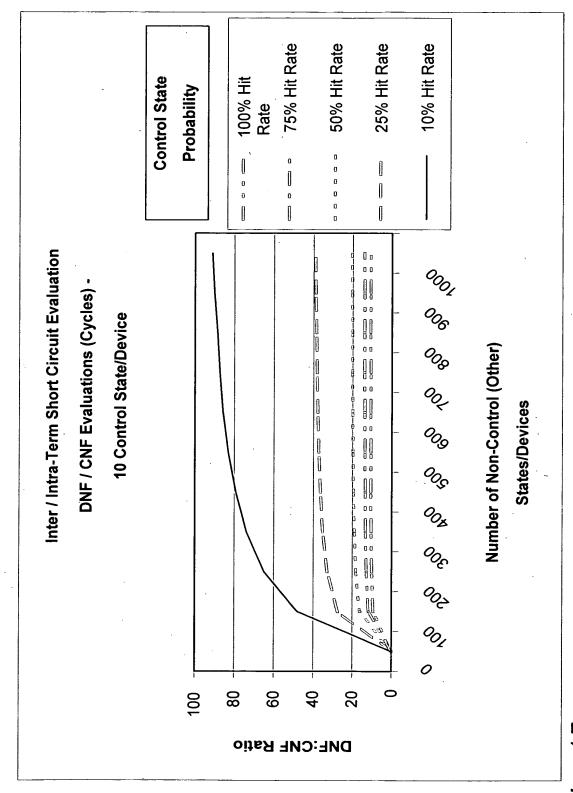


Fig. 15

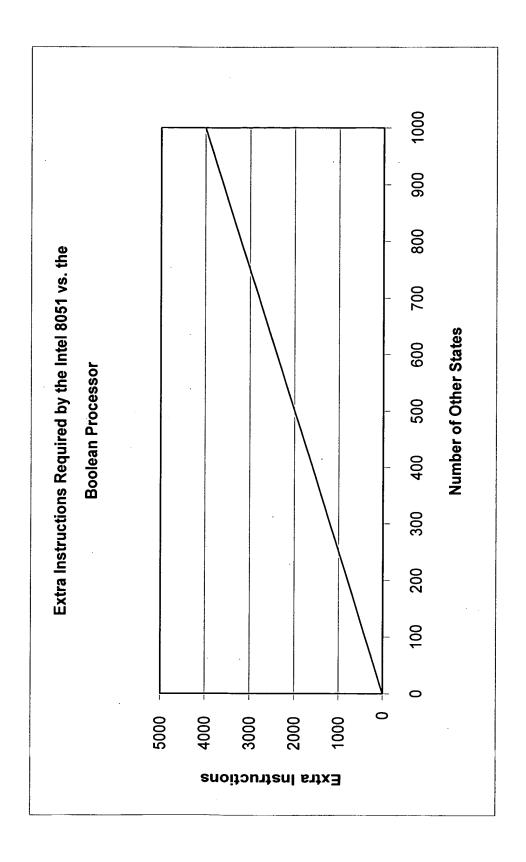


Fig. 16

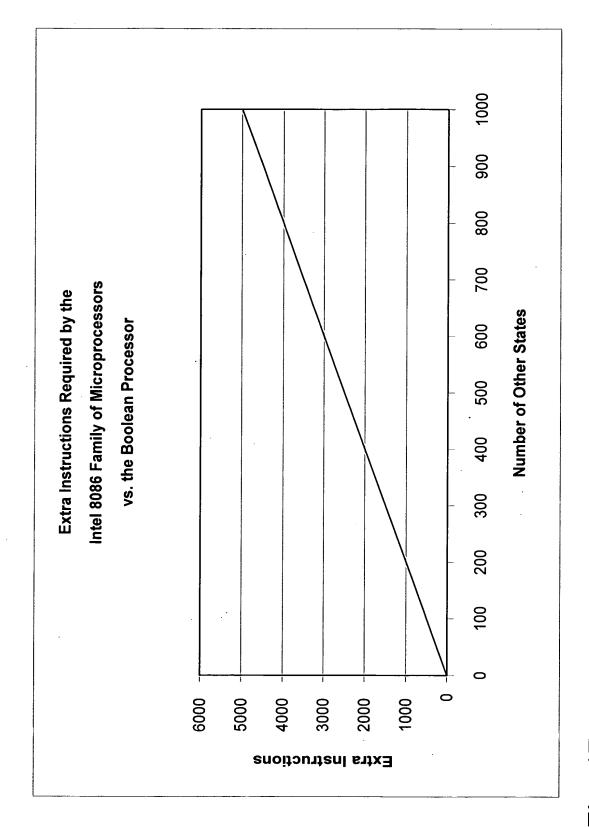
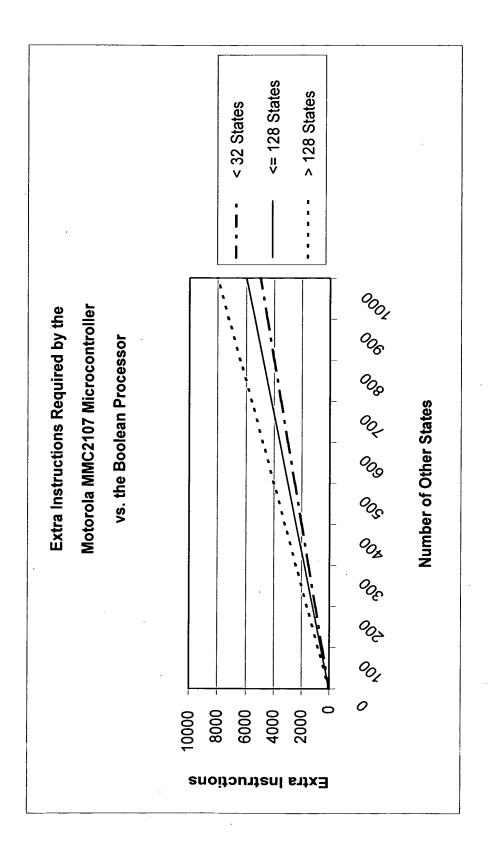


Fig. 17



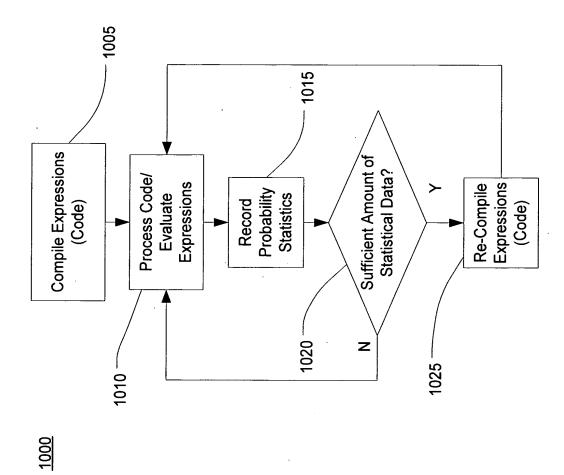
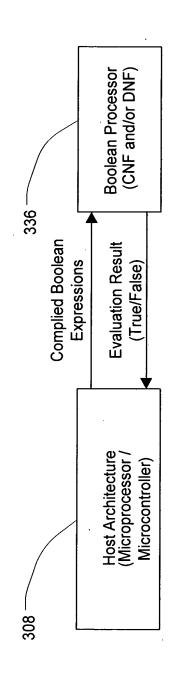


Fig. 19



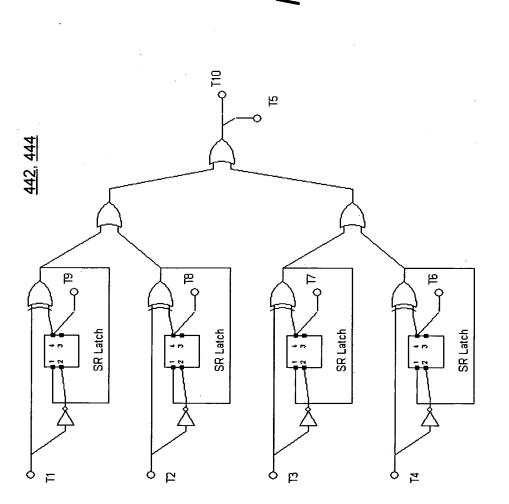
Changes State Boolean Processor (CNF and/or DNF) Device(s) Device State(s) Complied Boolean **Evaluation Result** Expressions (True/False) Host Architecture (Microprocessor / Microcontroller) 308

336

Fig. 20

Fig. 21

Fig. 22



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72 O-Reset

437, 439, 454, 458

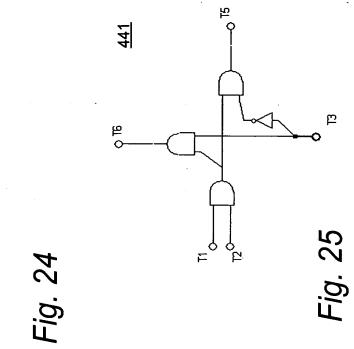
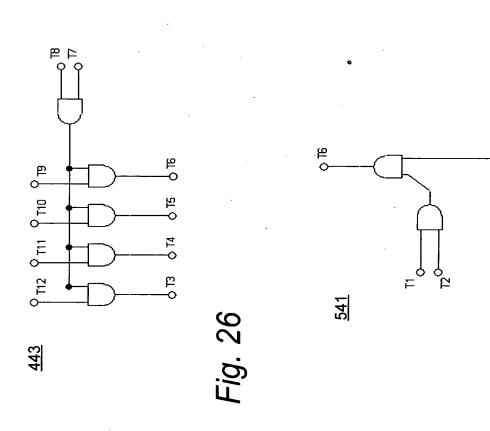


Fig. 23



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Fig. 27

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Fig. 29

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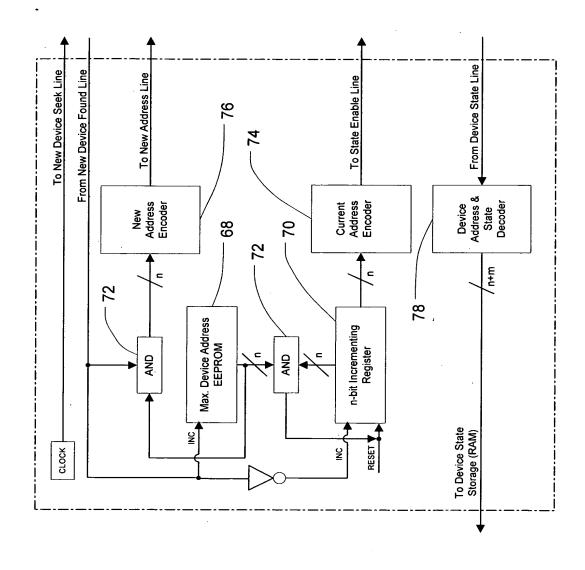
20

541

536

Fig. 28

Fig. 30



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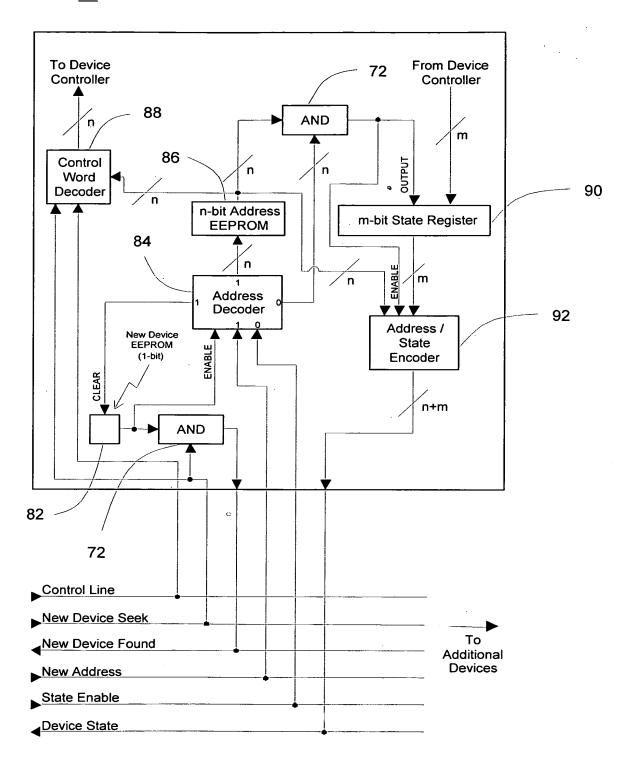


Fig. 32

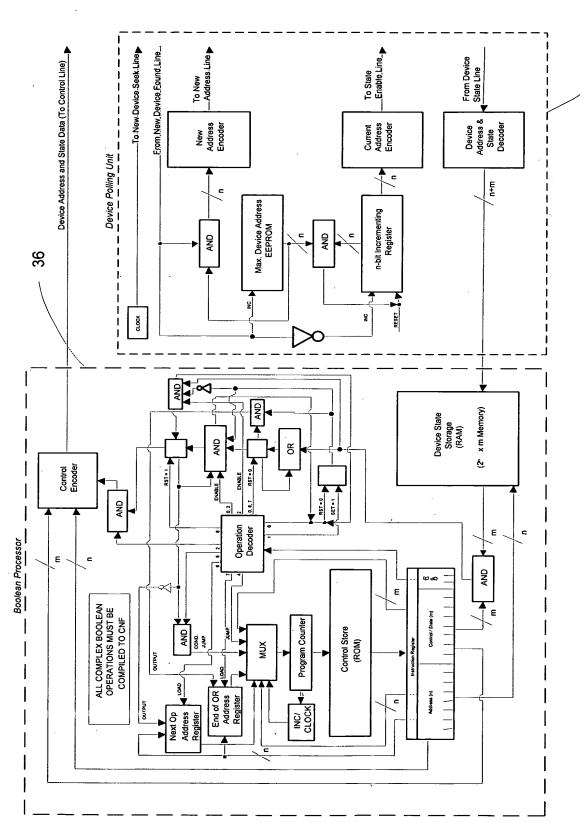


Fig. 33

99

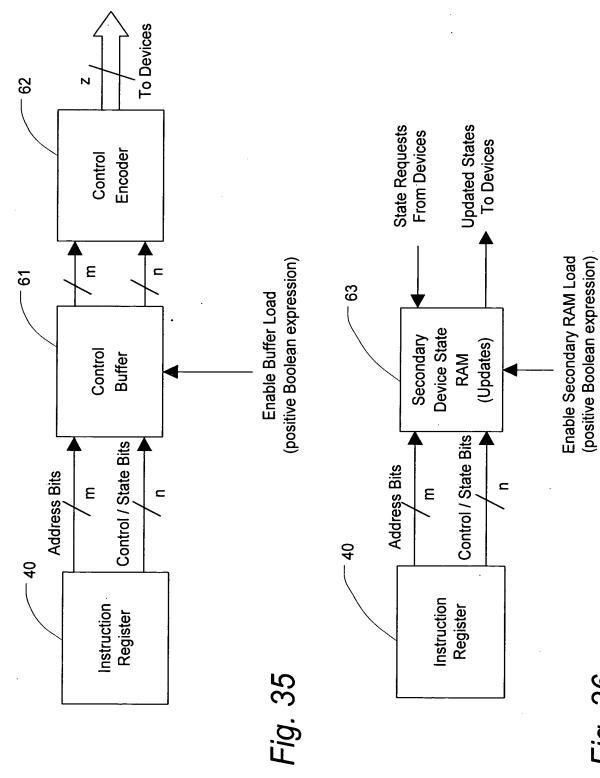


Fig. 36

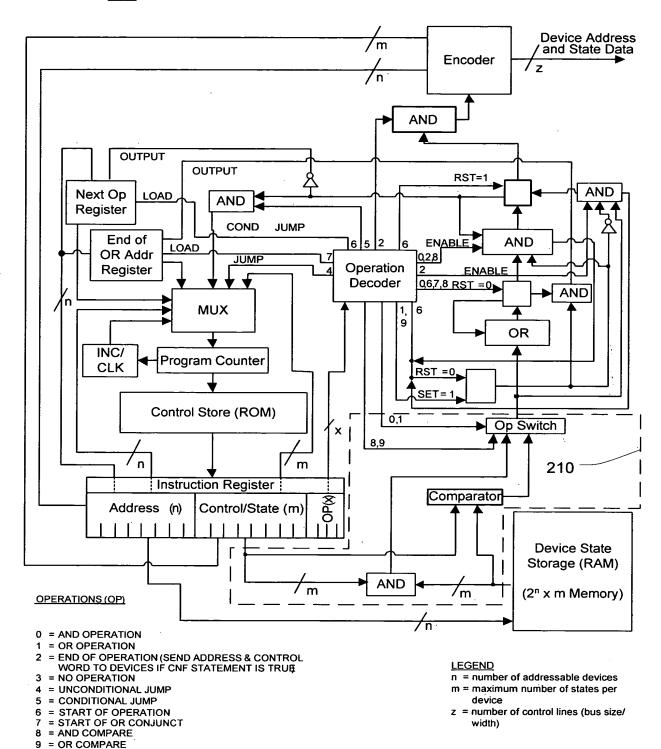


Fig. 37

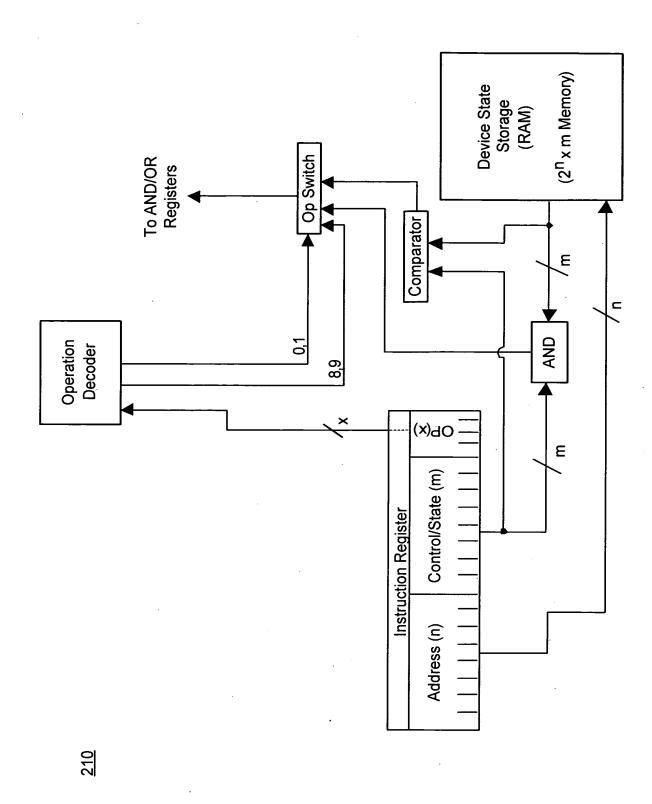


Fig. 38

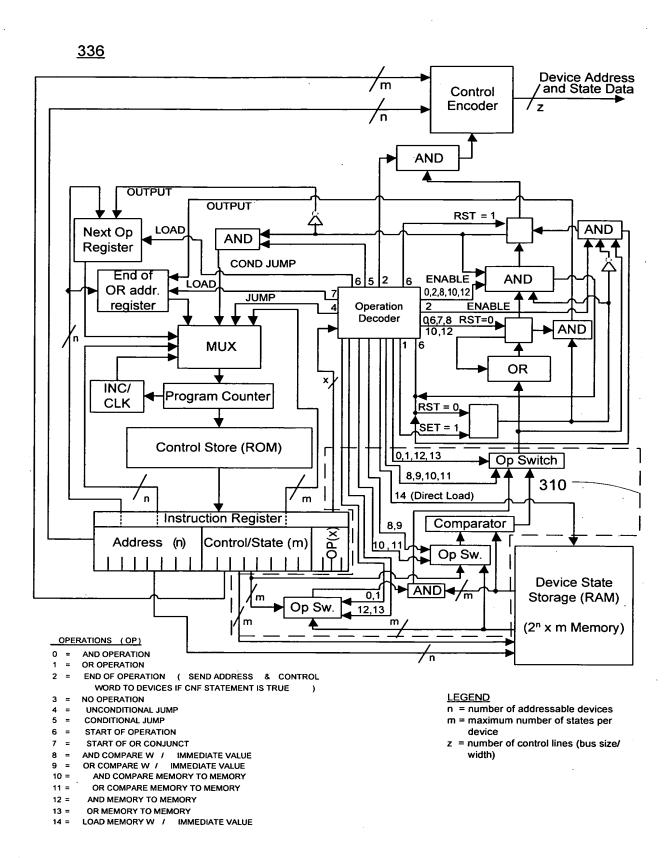
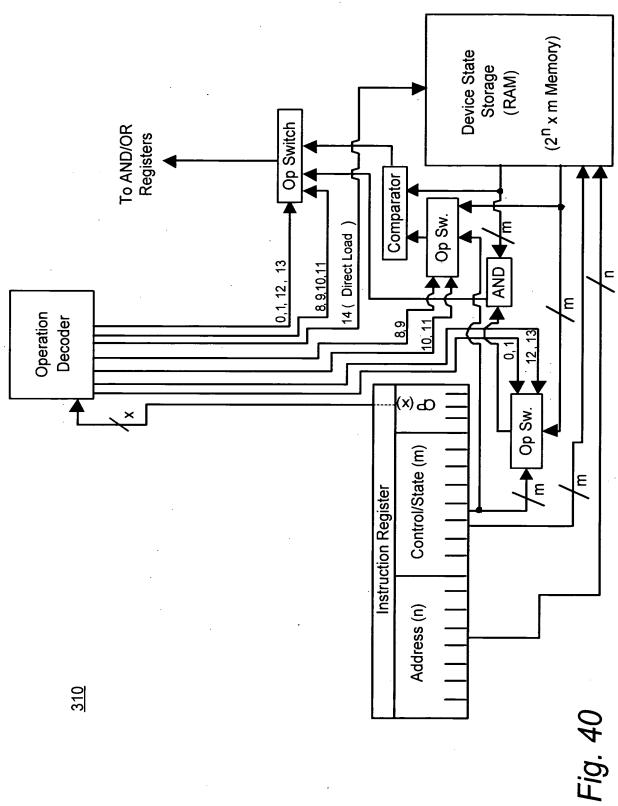


Fig. 39



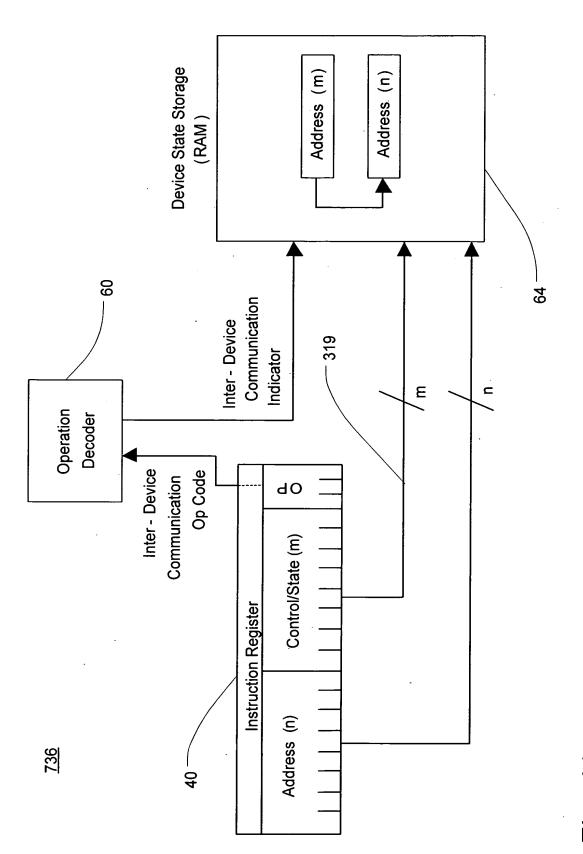


Fig. 41

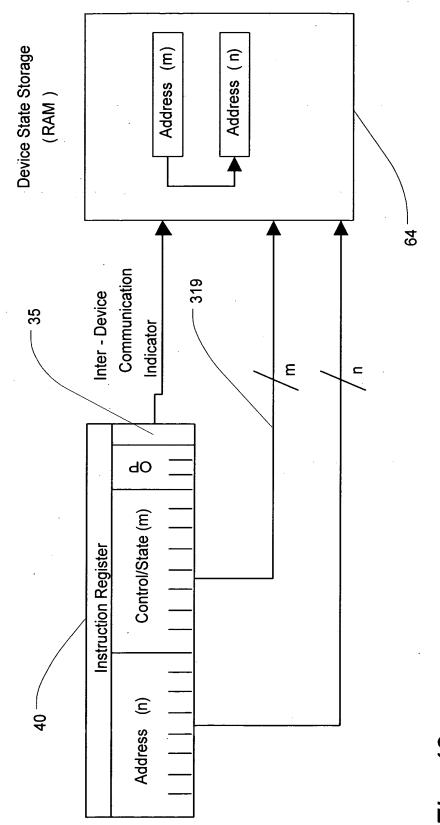


Fig. 42

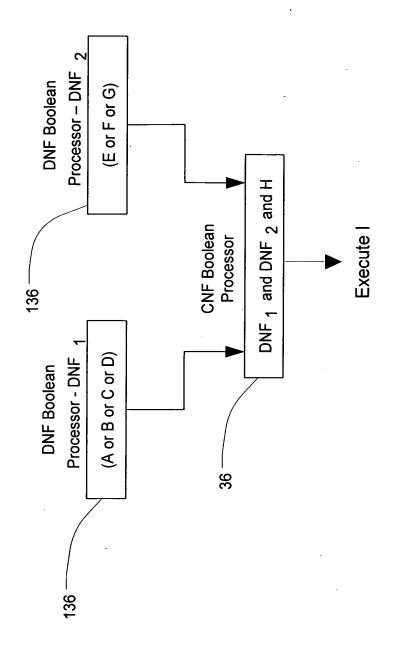


Fig. 43